REMARKS

Claims 1 - 23, 25 - 27, 29 - 35, 37, 38 and 42 - 45 are pending in the above-identified application. Claims 1 - 19 are withdrawn from consideration.

In the Office Action of August 14, 2003, Claims 20 - 23, 25 - 27, 29 - 35, 37, 38 and 42 - 45 were rejected. No claim was allowed. In response, Claims 20, 21, 32 - 35, 37, 38 and 42 - 45 are amended and Claims 1 - 19 and 22 - 31 are canceled without prejudice or disclaimer.

Reexamination and reconsideration are respectfully requested in view of the foregoing amendments and the following remarks.

Objection to the Title

The Examiner alleged that the title is not descriptive. In response, the title is amended to be directed to a fabrication method only and not to a device and method. It is respectfully submitted that the Examiner's objection to the title is thereby overcome.

Objection to the Claims

The Examiner objected to Claims 21 - 23, 25 - 27, 29, 35, 37 - 38 and 42 - 45 because of informalities. In response, claims 21, 32 - 35, 37 - 38 and 42 - 45 are amended to recite "The method of fabrication a semiconductor". (Claims 22 - 23 and 25 - 27 are canceled). It is respectfully submitted that the Examiner's objection to the claims is thereby overcome.

The Invention

The invention as set forth in the amended claims is a method of fabricating a semiconductor integrated circuit device having damascene type interconnections with thin conducting barrier films and pure copper wiring, where a pure copper seed film is used to obtain a pure copper interconnection prior to electroplating, and an ammonia plasma treatment is performed to remove the remaining damage and surface contamination to reduce the impurity degradation of the copper wiring through the following plasma CVD.

Rejection of Claims 20, 25 - 27, 29 - 35, 37 - 38 and 42 - 45 under 35 U.S.C. §103(a) over Edelstein in view of Kaufman and further in view of Lai

Claims 20, 25 - 27, 29 - 35, 37 - 38 and 42 - 45 are rejected under 35 U.S.C. §103(a) as being obvious over Edelstein et al (U.S. Patent No. 6,181,012) in view of Kaufman et al (U.S. Patent No. 6,593,239) and further in view of Lai (U.S. Patent No. 6,136,680). The Examiner alleges that Edelstein discloses a method of fabricating a semiconductor integrated circuit device comprising providing a semiconductor substrate having a first main surface, forming a first insulating film over the first main surface of the semiconductor substrate, forming an embedded interconnection slot in the first insulating film over the main surface, forming a connecting hole in a bottom surface of the embedded interconnection slot, connected to a lower conducting layer, forming a conducting barrier film over a surface region of the first insulating film outside the embedded interconnection slot and the connecting hole and the bottom surface and side surface of the embedded interconnection slot and the connecting hole, forming a metal film having copper as its main component over the conducting barrier film so as to fill the embedded interconnection slot and the connecting hole, removing the metal film outside the embedded interconnection slot and the

connecting hole by a chemical mechanical polishing method to form an embedded metal interconnection layer having copper as its main component embedded in the interconnection slot and in the connecting hole in which the conducting barrier film is formed, and forming a cap insulating film so as to cover the embedded metal interconnection layer and the upper surface of said first insulating film, wherein the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor integrated circuit device does not exceed 0.8At%, and the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is about 10 nm. The Examiner acknowledges that Edelstein does not disclose a CMP method using a polishing slurry containing an oxidizing agent of copper and organic acid capable of dissolving an oxide of copper within a corrosion region of copper. The Examiner alleges that Kaufman discloses a CMP method using a polishing slurry containing an oxidizing agent of copper and organic acid capable of dissolving an oxide of copper within a corrosion region of copper. The Examiner takes the position that it would have been obvious to polish the semiconductor device of Edelstein by using a polishing slurry containing an oxidizing agent of copper and organic acid as taught by Kaufman in order to prevent surface damage to the first insulating film and the metal film. The Examiner acknowledges that Edelstein and Kaufman do not teach the thickness of the conducting barrier film, but alleges that it would have been obvious to form the conducting barrier film having a desired thickness. The Examiner further acknowledges that Edelstein and Kaufman do not disclose that the first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner alleges that Lai discloses that a metal film is planarized

by chemical mechanical polishing and that a first main surface of the semiconductor substrate is plasma treated in an atmosphere of a gas having reducing properties prior to forming a cap insulating film. The Examiner takes the position that it would have been obvious to plasma treat the first main surface of the semiconductor substrate of Edelstein and Kaufman in an atmosphere of a gas having reducing properties prior to forming a cap insulating film as taught by Lai in order to suppress hillocks formation.

Regarding Claims 25 - 27, the Examiner alleges that Edelstein, Kaufman and Lai disclose that the gas atmosphere comprises hydrogen and/or nitride hydride as its principal component element.

Regarding Claims 29-31, 37 - 38 and 42, the Examiner takes the position that although Edelstein, Kaufman and Lai do not teach the exact mass ratio of abrasive particles, it would have been obvious to form the circuit having the desired mass ratio of abrasive particles as involving only routine skill in the art.

Regarding Claims 43-45, the Examiner alleges that Edelstein, Kaufman and Lai disclose that the width of the embedded interconnection slot does not exceed 0.4 μm (less than 0.5 μm).

This rejection is respectfully traversed as it may apply to the amended claims. In particular, independent Claim 20 is amended to include the features that a pure copper seed film is used to obtain a pure copper interconnection prior to electroplating, and an ammonia plasma treatment is performed to remove the remaining damage and surface contamination to reduce the impurity degradation of the copper wiring through the following plasma CVD. The limitations are supported, for example by Figs. 66 to 77 and the corresponding description in the specification. Edelstein discloses a dual damascene process wherein an impurity-doped copper

seed film (not pure seed) is deposited prior to a main copper film deposition so as to improve electromigration resistance, adhesion and other surface properties of the damascene interconnection. Edelstein does not disclose or suggest any pure copper seed sputtering with a target that is 99.9999% or more pure. In fact, Edelstein teaches away from using pure copper, specifying that the seed layer in its method is a copper alloy or another metal that does not contain copper (see, for example, col. 7, line 51 to col. 9, line 39 of the reference). Neither Kaufman nor Lai supply the missing feature from Edelstein. Kaufmann relates only to CMP processes. Lai relates only to ammonia plasma treatment after CMP processes for copper damascene.

Accordingly, the combination of Edelstein, Kaufmann and Lai does not teach or suggest the present invention.

Further, it is respectfully submitted that the claimed invention would not be obvious over the combination of Edelstein, Kaufmann, Lai and Maekawa. As discussed below, Maekawa has been cited by the Examiner as allegedly teaching forming a metal film by sputtering using a target wherein the purity of copper is not less than 99.999%. As discussed above, independent Claim 20 of the present invention is amended herein to contain a feature of forming a copper seed layer by copper sputtering with a copper target having its purity of 99.999% or more. Maekawa discloses a method that includes a step of forming a copper film by deposition with a pure copper target, but the reference does not disclose or suggest any copper seed processes for copper electroplating. In fact, Maekawa is directed to a process of filling up interconnection grooves by copper sputtering without electroplating. Therefore, Maekawa would not have provided any motivation to use pure copper in forming a seed layer. Accordingly, the process of independent Claim 20 would not have been obvious over Maekawa and Edelstein.

Accordingly, it is respectfully submitted Claims 20, 32 - 35, 37 - 38 and 42 - 45 would not have been obvious over Edelstein, Kaufmann, Lai or Maekawa, alone or in combination (Claims 25 - 27 and 29 - 31 are canceled).

Rejection of Claims 21 - 23 under 35 U.S.C. §103(a) over Edelstein in view of Kaufman and Lai and further in view of Maekawa

Claims 21 - 23 are rejected under 35 U.S.C. §103(a) as being obvious over Edelstein in view of Kaufman and Lai and further in view of Maikawa (U.S. Patent No. 6,171,957). The Examiner alleges that Edelstein, Kaufman and Lai disclose all of the claimed limitations except that the metal film is formed by sputtering using a target wherein the purity of copper is not less than 99.999%. The Examiner alleges that Maekawa discloses forming a metal film by sputtering using a target wherein the purity of copper is not less than 99.999%. The Examiner takes the position that it would have been obvious to form the metal film of Edeistein, Kaufman and Lai by sputtering using a target wherein the purity of copper is not less than 99.999%, such as taught by Maekawa in order to reduce the resistance of the metal film.

Regarding claims 21 and 23, The Examiner alleges that Edelstein, Kaufman, Lai and Maekawa disclose copper having purity of 99.999 wt% or higher. The Examiner acknowledges that Edelstein, Kaufman, Lai and Maekawa do not disclose copper having purity of 99.9999 wt%. The Examiner takes the position that it would have been obvious to form the copper having purity of 99.9999 wt% in order to produce the small line width and to increase the speed of the device to meet the performance goal.

This rejection is respectfully traversed as it may apply to the amended claims. As discussed above, independent Claim 20 includes the features that a pure copper

seed film is used to obtain a pure copper interconnection prior to electroplating. Edelstein, on the other hand, requires impure copper or a metal that does not contain copper for its seed layer. The disclosure in Maekawa of the deposition of pure copper in a fabrication process does not relate to the formation of a seed layer prior to electroplating.

Accordingly, it is respectfully submitted Claim 21 would not have been obvious over Edelstein, Kaufman, Lai or Maekawa, alone or in combination (Claims 22 - 23 are canceled).

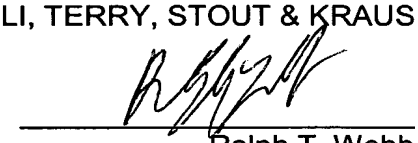
Conclusion

In view of the foregoing amendments and remarks, it is respectfully submitted that Claims 20 - 21, 32 - 35, 37 - 38 and 42 - 45 are in condition for allowance. Favorable reconsideration is respectfully requested.

Should the Examiner believe that anything further is necessary to place this application in condition for allowance, the Examiner is requested to contact applicants' undersigned attorney at the telephone number listed below.

Kindly charge any additional fees due, or credit overpayment of fees, to Deposit Account No. 01-2135 (501.39932X00).

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS



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